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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,755	DI GREGORIO, LORENZO	
	Examiner	Art Unit	
	Nima Mahmoudzadeh	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24,27,28,30-33,38 and 39 is/are rejected.

7)☒ Claim(s) 25,26,29 and 34-37 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04/15/2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 06/14/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 9, 24, 27, 28, 30 - 32, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vila et al. (US Patent No. 6,757,348) in view of Gaither et al. (US Patent Publication No. 2003/0084250)

Regarding claim 1, Vila et al. teach a scheduler for a memory system for buffer storage of data processed by at least one data processing unit, comprising:

a write unit for writing data objects to the memory system, said write unit:

receiving data (Column 3, lines 59-61) packets from at least one data source at a variable data (Column 3, lines 59-61) transmission rate, the data packets having payload data;

calculating attribute data (Fig.6 & 7) for each received data packet;

writing the data (Column 4, lines 10-11) contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data (Column 6, lines 63-67) for linking the data objects (Column 4, 26-32), the attribute data calculated, and the payload data; and

inserting filling objects (Column 6, lines 1-5) into the memory system between the data objects linked to one another to compensate for the variable data transmission rate (Column 3, lines 59-61) when writing (Column 4, lines 10-11) the data object string to the memory system.

Vila et al. do not teach a counter connected to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects; and

a time out signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored in the memory system is ready to be read; and

subsequently decrementing said counter corresponding to the data contained in the data object provided.

However, Gaither et al. teach a counter connected (Paragraph [0023]) to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects; and

a time out (Wait period acts as time out function. Paragraph [0034]) signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value (Paragraph [0028]), to the data processing unit that at least one of the data object and the

filling object buffer-stored (Paragraph [0035]) in the memory system is ready to be read; and

subsequently decrementing (Fig. 4c, 416) said counter corresponding to the data contained in the data object provided.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing of Vila et al. to include a increment/decrement counter and signaling, when said counter reaches a threshold value taught by Gaither et al. in order to use the memory capacity of the memory system as efficiently as possible and signal the available data packets with very good time accuracy.

Regarding claim 2, Vila et al. teach the scheduler according to claim 1, wherein the data object string (Column 6, lines 49-52) includes linked data objects (Column6, lines 49-52) having different data object types.

Regarding claim 9, Vila et al. teach the scheduler according to claim 1, wherein said write unit has a control path (Fig. 9) and a data path (Fig. 9).

Regarding claim 24, Vila et al. teach the scheduler according to claim 9, wherein said data path has a counting device incremented linearly in accordance with a linear nominal data arrival curve (Fig. 2B).

Regarding claim 27, Vila et al. teach the scheduler according to claim 9. Vila et al. fail to teach the scheduler wherein:

said data path has a basic address register bank including at least two basic address registers; and

one of said basic address registers is provided for each data source. However, Gaither et al teach a system wherein:

said data path has a basic address register bank including at least two basic address registers (Paragraph [0036], lines 18-22); and

one of said basic address registers is provided for each data source (Paragraph [0036], lines 18-22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing which is provided for each data source of Vila et al. to include a basic address register bank and basic address registers which is provided for each data source taught by Gaither et al. in order to use the memory capacity of the memory system as efficient as possible and signal the available data packets with very good time accuracy.

Regarding claim 28, Vila et al. teach the scheduler according to claim 9. Vila et al. fail to teach the scheduler wherein:

the data source is a plurality of data sources;

said data path has a basic address register bank including at least two basic address registers; and

one of said basic address registers is provided for each of said data sources.

However, Gaither et al teach, a system wherein:

the data source is a plurality of data sources;

said data path has a basic address register bank including at least two basic address registers (Paragraph [0036] lines 18-22); and

one of said basic address registers is provided for each of said data sources (Paragraph [0036]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing which is provided for each data source of Vila et al. to include a basic address register bank and basic address registers which is provided for each data source taught by Gaither et al. in order to use the memory capacity of the memory system as efficient as possible and signal the available data packets with very good time accuracy.

Regarding claim 30, Vila et al. teach the scheduler according to claim 9. Vila et al. fail to teach a system wherein:

said data path has a link address register bank including at least two link address registers; and

one of said link address registers is provided for each data source.

However, Gaither et al teach the scheduler according to claim 9, wherein:

said data path has a link address register bank including at least two link address registers (Paragraph [0036] , lines 18-22); and

one of said link address registers is provided for each data source (Paragraph [0036], lines 18-22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing which is provided for each data source of Vila et al. to include a basic address register bank and basic address registers which is provided for each data source taught by Gaither et al. in order to use the memory capacity of the memory system as efficient as possible and signal the available data packets with very good time accuracy.

Regarding claim 31, Vila et al. teach the scheduler according to claim 9. Vila et al. fail to teach a system wherein:

the data source is a plurality of data sources;

said data path has a link address register bank including at least two link address registers; and

one of said link address registers is provided for each of said data sources.

However, Gaither et al teach a system wherein:

the data source is a plurality of data sources (Paragraph [0036] , lines 18-22);

said data path has a link address register bank including at least two link address registers (Paragraph [0036] , lines 18-22); and

one of said link address registers is provided for each of said data sources (Paragraph [0036] , lines 18-22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing which is provided for each data source of Vila et al. to include a basic address register bank and basic address registers which is provided for each data source taught by Gaither et al. in order to use the memory capacity of the memory system as efficient as possible and signal the available data packets with very good time accuracy.

Regarding claim 32, Vila et al. teach the scheduler according to claim 30. Vila et al. fail to teach the system wherein said link address register buffer-stores an address of the data object written most recently to the memory system for linking to a next data object in the data object string.

However, Gaither et al teach a system wherein said link address register buffer-stores an address of the data object written most recently to the memory system for linking to a next data object in the data object string (Paragraph [0035]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing of Vila et al. to store address of the data object in the buffer taught by Gaither et al. in order for the memory system to link to a next data object in the data object string.

Regarding claim 38, Vila et al. teach in a data processing device having at least one data source, a memory system, and at least one data processing unit, a scheduler for buffer storing data processed by the data processing unit, the scheduler comprising:

a write unit writing data objects to the memory system, said write unit:

receiving data (Column 3, lines 59-61) packets from the at least one data source at a variable data (Column 3, lines 59-61) transmission rate, the data packets having payload data;

calculating attribute data (Fig. 6 & 7)for each received data packet;

writing the data (Column 4, lines 10-11) contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data (Column 6, lines 63-67) for linking the data objects (Column 4, 26-32), the attribute data calculated, and the payload data; and

inserting filling objects (Column 6, lines 1-5) into the memory system between the data objects linked to one another to compensate for

the variable data transmission rate (Column 3, lines 59-61) when writing (Column 4, lines 10-11) the data object string to the memory system.

Vila et al. fail to teach a counter connected to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects; and

a time out signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored (Paragraph [0035]) in the memory system is ready to be read; and subsequently decrementing said counter corresponding to the data contained in the data object provided.

However, Gaither et al. teach a counter connected (Paragraph [0023]) to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects; and

a time out (Wait period acts as time out function. Paragraph [0034]) signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value (Paragraph [0028]), to the data processing unit that at least one of the data object and the filling object buffer-stored ([Paragraph [0035]) in the memory system is

ready to be read; and subsequently decrementing (Fig. 4c, 416) said counter corresponding to the data contained in the data object provided.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing of Vila et al. to include a increment/decrement counter and signaling, when said counter reaches a threshold value taught by Gaither et al. in order to use the memory capacity of the memory system as efficiently as possible and signal the available data packets with very good time accuracy.

Regarding claim 39, Vila et al. teach in a data processing device having at least one data source, a memory system, and at least one data processing unit, a scheduler for buffer storing data processed by the data processing unit, the scheduler comprising:

a counter;

a write unit for writing data objects to the memory system, said write unit connected to said counter and being programmed to:

receive data (Column 3, lines 59-61) packets from the at least one data source at a variable data (Column 3, lines 59-61) transmission rate, the data packets having payload data;

calculate attribute data (Fig. 6 & 7) for each received data packet;

write the data (Column 4, lines 10-11) contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data (Column 6, lines 63-67) for linking the data objects (Column 4, 26-32), the attribute data calculated, and the payload data; and

compensate for the variable data transmission rate when writing the data object string to the memory system by inserting filling objects (Column 6, lines 1-5) into the memory system between the data objects linked to one another; and

Vila et al. fail to teach increment said counter to correspond to an amount of data contained in the data packet and the filling data in the filling objects when the data object string is written to the memory system;

a time out signaling unit connected to said counter, said time out signaling unit being programmed to:

signal, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored (Paragraph [0035]) in the memory system is ready to be read; and

subsequently decrement said counter corresponding to the data contained in the data object provided.

However, Gaither et al. teach increment said counter (Paragraph [0023]) to correspond to an amount of data contained in the data packet and the filling data in the filling objects when the data object string is written to the memory system;

a time out (Wait period acts as time out function. Paragraph [0034]) signaling unit connected to said counter, said time out signaling unit being programmed to:

signal, when said counter reaches a threshold value (Paragraph [0028]), to the data processing unit that at least one of the data object and the filling object buffer-stored (Paragraph [0035]) in the memory system is ready to be read; and

subsequently decrement (Fig. 4c, 416) said counter corresponding to the data contained in the data object provided.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer management and memory addressing of Vila et al. to include a increment/decrement counter and signaling, when said counter reaches a threshold value taught by Gaither et al. in order to use the memory capacity of the memory system as efficiently as possible and signal the available data packets with very good time accuracy.

3. Claims 3 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vila et al. (US Patent No. 6,757,348) in view of Gaither et al. (US Patent Publication No. 2003/0084250) and further in view of Yu (US Patent Application No. 2005/0063396).

Regarding claim 3, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach the scheduler wherein a first of said data object types is a string start data object having:

a type data field for identification as the string start data object;

a transmission flag;

a pointer data field for linking;

an attribute data field; and

a payload data field .

However, Yu teaches a type data field for identification (Fig. 17, TT and paragraph [0342]) as the string start data object (Paragraph [0266] & Fig. 17);

a transmission flag (Paragraph [0266]);

a pointer data field for linking (Fig. 178, FWR/SWR);

an attribute data field (Fig. 17); and

a payload data field (Fig. 17).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer framing of Vila et al. in view of Gaither et al. include frame addressing taught by Yu in order to have different types of data field and frames.

Regarding claim 4, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach a system wherein a second of said data object types is a string end data object having:

a type data field for identification as the string end data object; and

a data field for inputting an amount of the payload data; and

a payload data field.

However, Yu teaches a scheduler wherein a second of said data object types is a string end data object having (Paragraph [0266]):

a type data field for identification (Fig. 17, TT) as the string end data object;

a data field for inputting (fig. 5, Tributary TX framer) an amount of the payload data (Fig. 17); and

a payload data field (Fig. 17).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer framing of Vila et al. in view of Gaither et al. to include frame addressing taught by Yu in order to have different types of data field and frames.

Regarding claim 5, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach a system

wherein a third of said data object types is a string end and start data object having:

a type data field for identification as the string end and start data object;

a data field for outputting the amount of payload data; and

a transmission flag; an attribute data field; and

a payload data field.

However, Yu teaches a system wherein a third of said data object types is a string end and start data object having (Paragraph 0266]):

a type data field for identification as the string end and start data object (Paragraph [0266]);

a data field for outputting the amount of payload data (Fig. 17, U/M/B);

a transmission flag (Paragraph [0266]); and

an attribute data field (Fig. 17); and

a payload data field (Fig. 17).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer framing of Vila et al. in view of Gaither et al. to include frame addressing taught by Yu in order to have different types of data field and frames.

Regarding claim 6, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach a system wherein a fourth of said data object types is a string center data object having:

a type data field for identification as the string center data object; and

a pointer data field; and

a payload data field.

However Yu teaches a system wherein a fourth of said data object types is a string center data object having (Fig. 17, destination address and payload):

a type data field for identification as the string center data object (Paragraph [0266] and Fig. 17);

a pointer data field (Fig. 17, FWR/SWR); and

a payload data field (Fig. 17).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer framing of Vila et al. in view of Gaither et al. to include frame addressing taught by Yu in order to have different types of data field and frames.

Regarding claim 7, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach a system wherein a fifth of said data object types is a single-byte filling object having a type data field including one byte for identification as a single-byte filling object.

However, Yu teaches a system wherein a fifth of said data object types is a single-byte filling object (Paragraph [0360] and Fig. 17) having a type data field including one byte for identification as a single-byte filling object (Paragraph [0360] and Fig. 17).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer frame structure of Vila et al. in view of Gaither et al. to include identification byte taught by Yu in order to have different types of data field and frames.

Regarding claim 8, Vila et al. in view of Gaither et al. teach the scheduler according to claim 2. Vila et al. in view of Gaither et al. fail to teach a system wherein a sixth of said data object types is a multiple-byte filling object having a type data field for identification as a multiple byte filling object and a data field indicating an amount of filling data.

However, Yu teaches a system wherein a sixth of said data object types is a multiple-byte filling object (Paragraph [0360] and Fig. 17) having a type data field for identification as a multiple byte filling object and a data field (Paragraph [0360] and Fig. 17) indicating an amount of filling data.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer frame structure and type of Vila et al. in view of Gaither et al. to include a type data field for identification taught by Yu in order to have multiple-byte filling object as a sixth of said data object type.

4. Claims 10, 11, 14- 17, 21- 23, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vila et al. (US Patent No. 6,757,348) in view of Gaither et al. (US Patent Publication No. 2003/0084250) further in view of Ebergen (US Patent No. 6,700,825)

Regarding claim 10, Vila et al. in view of Gaither et al. teach the scheduler according to claim 9. Vila et al. in view of Gaither et al. fail to teach the scheduler wherein said data path has:

a FIFO memory; and

a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory.

However, Ebergen teaches a system wherein said data path has:
a FIFO memory (Column 1, lines 38-42); and
a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory (Column 2, lines 30-43).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory features of Vila et al. in view of Gaither et al. to include FIFO memory read, write, buffer storage and FIFO control data taught by Ebergen in order to have variations of FIFO control and buffer interaction.

Regarding claim 11, Vila et al. in view of Gaither et al. teach the scheduler according to claim 10. Vila et al. in view of Gaither et al. fail to teach a system wherein said FIFO control unit receives data from the at least one data source in the form of packets as data packets.

However, Ebergen teaches a system wherein said FIFO control unit receives data from the at least one data source in the form of packets as data packets (Column 3, lines 19-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the buffer structure of Vila et al. in view of Gaither et al. to receive FIFO control data from a data source taught by Ebergen in order to have variations of FIFO control.

Regarding claim 14, Vila et al. in view of Gaither et al. teach the scheduler according to claim 10. Vila et al. in view of Gaither et al. fail to teach a system wherein said FIFO control unit calculates attribute data for each received data packet.

However, Ebergen teaches a system wherein said FIFO control unit calculates attribute data for each received data packet (Column 2, lines 63-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory control frame structure of Vila et al. in view of Gaither et al. to calculate attribute data for each

received data packet taught by Ebergen in order to have variations of FIFO control.

Regarding claim 15, Vila et al. teach the scheduler according to claim 14, wherein:

the payload data in the received data packets respectively include administration data (Fig. 9, 101); and

said control path calculates the attribute data as a function of system settings of said write unit and of the administration data in the data packets (Column 10, lines 33-40).

Regarding claim 16, Vila et al. in view of Gaither et al. teach the scheduler according to claim 14. Vila et al. in view of Gaither et al. fail to teach a system wherein:

said FIFO memory has an attribute data buffer; and

said FIFO control unit buffer-stores the calculated attribute data in said attribute data buffer.

However, Ebergen teaches a system wherein:

said FIFO memory has an attribute data buffer (Column 3, lines 9-15); and

said FIFO control (Fig. 2, c, c2, and c3) unit buffer-stores the calculated attribute data in said attribute data buffer (Fig. 2, d1, d2, and d3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory structure and characteristic of Vila et al. in view of Gaither et al. to include an attribute data buffer and it's storage in in FIFO control unit buffer taught by Ebergen in order to be able to store attribute data in said data buffer.

Regarding claim 17 Vila et al. in view of Gaither et al. the scheduler according to claim 10. Vila et al. in view of Gaither et al. fail to teach a system wherein:

said FIFO memory has a payload data buffer; and

said FIFO control unit buffer-stores the payload data in a data packet with said payload data buffer.

However, Ebergen teaches a system wherein:

said FIFO memory has a payload data buffer (Buffers are divided to different sections in regards to data information and control information. Fig. 2); and

said FIFO control unit buffer-stores the payload data in a data packet with said payload data buffer (Information is being stored in different parts of the data frame depending on their characteristics. Fig.2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory buffer of Vila et al. in view of Gaither et al. to include FIFO memory taught by Ebergen in order to have FIFO payload data buffer stored by FIFO control unit buffer.

Regarding claim 21, Vila et al. in view of Gaither et al. teach the scheduler according to claim 10. Vila et al. in view of Gaither et al. fail to teach a system wherein:

said control path transmits control signals to said FIFO control unit; and

said FIFO control unit writes the attribute data and the payload data of a data packet to the memory system in the form of a data object string including data objects linked to one another as a function of the control signals said FIFO control unit receives from said control path.

However, Ebergen teaches a system wherein:

said control path transmits control signals to said FIFO control unit (Fig.2, C1-C3); and

said FIFO control unit writes the attribute data and the payload data of a data packet to the memory system in the form of a data object string (Column 2, lines 15-17) including data objects linked to one another (Column 2, lines 25-43) as a function of the control signals said FIFO control unit receives from said control path (Fig.2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory buffer of Vila et al. in view of Gaither et al. to include FIFO memory taught by Ebergen in order to transfer control signals from control path to FIFO control unit.

Regarding claim 22, Vila et al. teach the scheduler according to claim 10, wherein said FIFO control unit records a cumulative amount of attribute data of the attribute data in a data packet (Column 1, lines 52-55).

Regarding claim 23, Vila et al. teach the scheduler according to claim 10, wherein said FIFO control unit records the cumulative amount of payload data of the payload data in a data packet (Column 1, lines 52-55).

Regarding claim 33, Vila et al. teach the scheduler according to claim 10, wherein said data path has a data multiplexer (Fig.3, 33 and Fig.5, 51) for writing data to the memory system (Fig.3, 34) and an address multiplexer for supplying an address to the memory system (Fig.3, 33 and Fig.5, 51).

5. Claims 12,13,18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vila et al. (US Patent No. 6,757,348) in view of Gaither et al. (US Patent Publication No. 2003/0084250) further in view of Yu (US Patent Publication No. 2005/0063396) and further in view of Ebergen (US Patent No. 6,700,825)

Regarding claim 12, Vila at el. in view of Gaither et al. further in view of Ebergen teach the scheduler according to claim 11. Vila et al. in view of Gaither et al. further in view of Ebergen fail to teach a system wherein each received data packet has:

a control data item identifying a start of the data packet; and

a control data item identifying an end of the data packet.

However, Yu teaches a system wherein each received data packet has:

a control data item identifying a start of the data packet (Paragraph [0266]); and

a control data item identifying an end of the data packet (Paragraph [0266]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer frame structure and type of Vila et al. in view of Gaither et al. further in view of Ebergen to include a identifying start and end data packet taught by Yu in order to identify control data start and end data packet.

Regarding claim 13, Vila at el. in view of Gaither et al. further in view of Ebergen teach the scheduler according to claim 12. Vila et al. in view of Gaither et al. further in view of Ebergen fail to teach a system wherein the payload data in the received data packets respectively include administration data and information data.

However, Yu teaches a system wherein the payload data in the received data (Paragraphs [0326] and [0327]) packets respectively include administration data and information data (Payload includes admin information data. Paragraph [0323]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify payload frame structure of Vila et al. in view of Gaither et al. further in view of Ebergen to include administration and information data taught by Yu in order to store admin and information data in the payload.

Regarding claim 18, Vila et al. in view of Gaither et al. further in view of Ebergen teach the scheduler according to claim 10. Vila et al. in view of Gaither et al. further in view of Ebergen fails to teach a system wherein said FIFO memory has an attribute data buffer and a payload data buffer for each data source.

However, Yu teaches a system wherein said FIFO memory has an attribute data buffer and a payload data buffer for each data source (FIFO has different frame structure and sections. Fig.2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer frame structure of Vila et al. in view of Gaither et al. further in view of Ebergen to include FIFO buffer frame taught by Yu in order to include an attribute data buffer and a payload data buffer for a data source.

Regarding claim 19, Vila et al. in view of Gaither et al. further in view of Ebergen teach the scheduler according to claim 10. Vila et al. in view of

Gaither et al. further in view of Ebergen fails to teach a system wherein: the data source is a plurality of data sources; and said FIFO memory has an attribute data buffer and a payload data buffer for each of the data sources.

However, Yu teaches a system wherein:

the data source is a plurality of data sources; and

said FIFO memory has an attribute data buffer and a payload data buffer for each of the data sources (Fig.2, D1-D3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify buffer frame structure Vila et al. in view of Gaither et al. further in view of Ebergen to include FIFO memory taught by Yu in order to have an attribute data buffer and a payload data buffer for the data sources.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vila et al. (US Patent No. 6,757,348) in view of Gaither et al. (US Patent Publication No. 2003/0084250) further in view of Yu (US Patent Publication No. 2005/0063396) and further in view of Ebergen (US Patent No. 6,700,825) and further in view of Kaganoi (US Patent No. 6,772,269).

Regarding claim 20, Vila et al. in view of Gaither et al. further in view of Yu and further in view of Ebergen teach the scheduler according to claim 18. Vila et al. teach in view of Gaither et al. further in view of Yu and further in view of Ebergen

fail to teach a system wherein said FIFO control unit produces an error signal when said payload data buffer associated with one data source is full and receives no further data.

However, Kaganoi teaches a system wherein said FIFO control unit produces an error signal (Column 10, lines 28-32) when said payload data buffer associated with one data source is full and receives no further data (Column 10, lines 28-32).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify memory management of Vila et al. in view of Gaither et al. further in view of Yu and further in view of Ebergen to include memory full notification taught by Kaganoi in order to send out notification that the buffer is full and no more data can be accepted until the memory is free.

Allowable Subject Matter

7. Claims 25, 26, 29, and 34-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Vila et al. (US Patent No. 6,757,348) teach Systems and methods for enabling

data transfers over communications links having a plurality of transmission lanes. In one embodiment, a system comprises a plurality of elastic buffers, each of which is coupled to one of the lanes in the communications link, and a buffer controller coupled to the buffers. Data is clocked into the elastic buffers using a first clock signal and is clocked out of the buffers by a second clock signal. The buffer controller is configured to monitor each of the buffers and to detect impending underflow or overflow conditions. In response to detect in one of these conditions, the buffer controller will cause the words to be added or deleted, respectively, to all of the elastic buffers rather than only the buffer in which the overflow/underflow condition was detected. However, prior art of record fail to teach or render obvious, alone or in combination, method of calculating a time wheel distribution as a function of a calculated cumulative amount of data and of a count produced by counting device in order to have a write unit with an effective data address generator that calculates a time wheel distribution as claimed in dependent claims 25, 26 and 36 in combination with all limitations in the respective independent claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Vila et al. (US Patent No. 6,757,348) teach Systems and methods for enabling data transfers over communications links having a plurality of transmission lanes. In one embodiment, a system comprises a plurality of elastic buffers, each of which is coupled to one of the lanes in the communications link, and a buffer controller coupled to the buffers. Data is clocked into the elastic buffers using a first clock signal and is clocked

out of the buffers by a second clock signal. The buffer controller is configured to monitor each of the buffers and to detect impending underflow or overflow conditions. In response to detect in one of these conditions, the buffer controller will cause the words to be added or deleted, respectively, to all of the elastic buffers rather than only the buffer in which the overflow/underflow condition was detected. However, prior art of record fail to teach or render obvious, alone or in combination, the limitations mentioned for the said multiplexer in order to write data and supplying an address to the memory system as claimed in dependent claims 34, 35, and 37 in combination with all limitations in the respective independent claims.

10. The following is a statement of reasons for the indication of allowable subject matter: Ebergen (US Patent No. 6,700,825) teaches a novel FIFO data structure in the form of a multi-dimensional FIFO. For a rectangular multi-dimensional FIFO, data items are received at an input of an N-row-by-M-column FIFO array of cells and transferred to an output, via a predetermined protocol of cell transfers, in the same order as received. Transfer rules or protocol are controlled by a control circuit implemented using asynchronous pipeline modules or a control circuit relying upon transition signaling. . However, prior art of record fails to teach or render obvious, alone or in combination, the limitations mentioned for the FIFO control unit in order to register a basic address when there is a change to the calculated cumulative amount of payload data as claimed in dependent claim 29 in combination with all limitations in the respective independent claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ho et al. (US Patent No. 5,500,943) teach Data processor with rename buffer and FIFO buffer for in-order instruction completion

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Q. Tieu can be reached on (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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